

## Integrate High-Performance Analog/Mixed-Signal Circuits

William Evans, Steve Svoboda, and Anthony Gribben

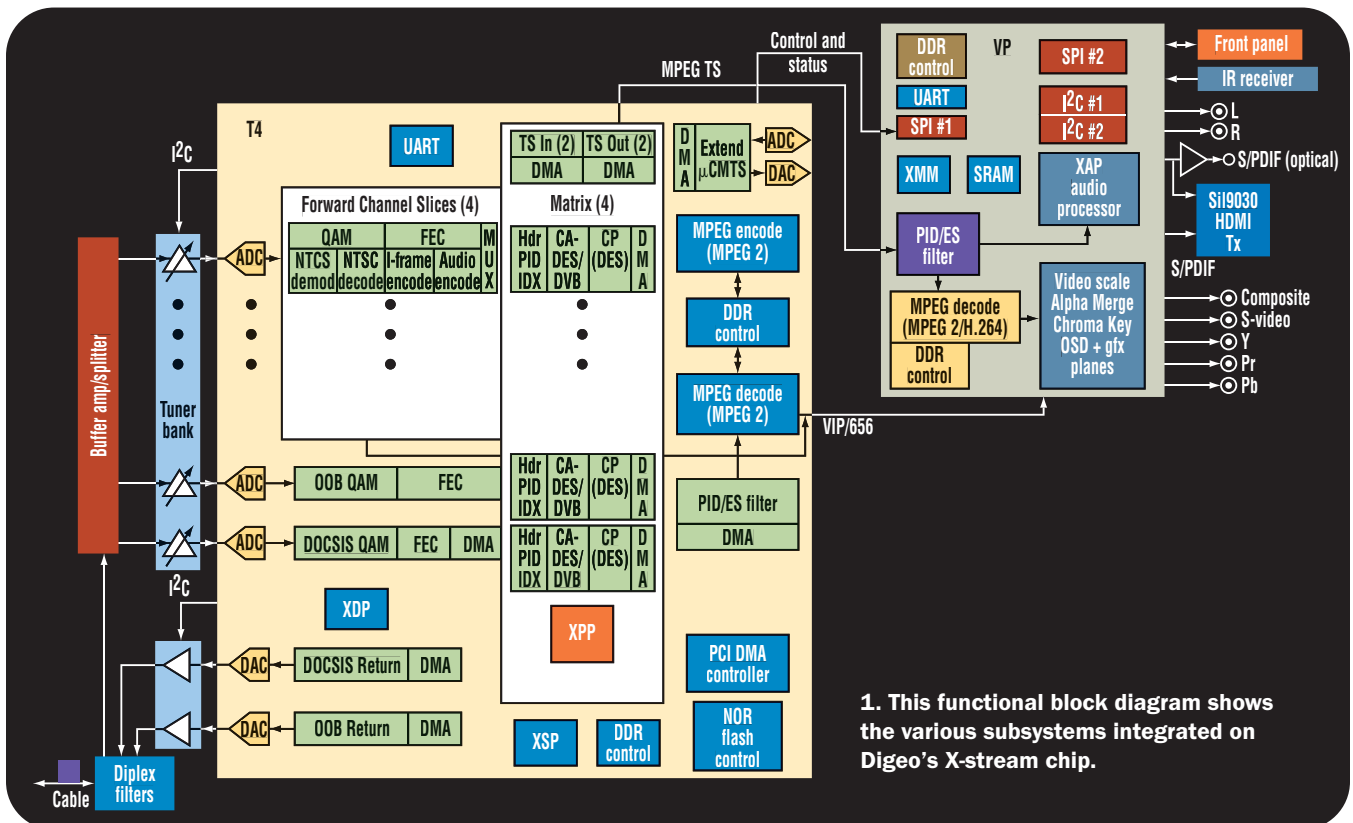
wpe@cadence.com, svoboda@cadence.com

Cadence Design Systems, Columbia, Md.

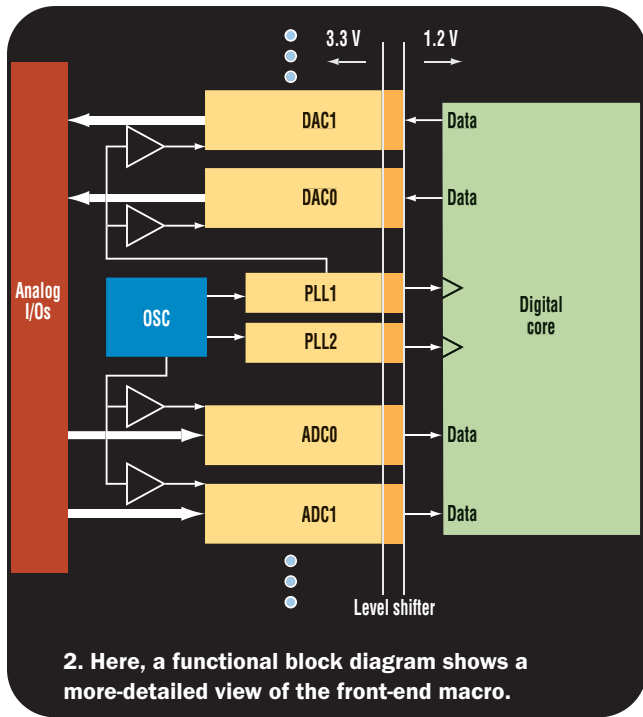
Interactive gaming consoles, digital TVs, and digital video recorders (DVRs), among other multimedia systems, benefit from higher levels of silicon integration. They achieve greater functionality, lower cost, better performance, and lower power consumption. In the many cases that call for very high-performance signal processing, silicon integration

becomes a critical enabler.

All of these multimedia systems have “front-ends” containing analog/mixed-signal subsystems for downstream demodulation and upstream modulation, which extensively use ADCs and DACs. Unfortunately, when placing multiple high-speed ADC and DAC chips on pc boards, the capacitances and



1. This functional block diagram shows the various subsystems integrated on Digeo's X-stream chip.



inductances (i.e. “parasitics”) present on the pc board and IC packages can severely degrade signal and timing integrity, causing crosstalk and other interference. Achieving the necessary channel-matching and isolation on a pc board for ultra-high-performance applications thus becomes extremely difficult.

This article describes various techniques for designing and integrating analog and mixed-signal components onto a single IC, using a project recently completed by engineers from Digeo Interactive and Cadence Design Systems as an example. The goal of the overall project was to develop a DVR chip set, called “X-stream,” using 130-nm 1.2-V/3.3-V standard CMOS logic. The X-stream chip set implements all of a four-video-tuner media center platform’s functions, including video-tuner interfaces, DOCSIS 2.0, out-of-band (OOB) processing, A/V codec, CableCARD, in-home A/V networking over coax, content/platform security, and graphics blending/scaling (Fig. 1). It only excludes host CPU, graphics rendering, USB 2.0, and SATA interfaces.<sup>1</sup>

To meet the stringent cost and signal-processing specifications for the X-stream chip set, the analog/mixed-signal front-end had to be integrated on-chip. This article details the design and integration of the analog/mixed-signal front-end, including the design of the ADCs, DACs, PLLs, and OSCs, along with the methods and tradeoffs that the team had to make to integrate these successfully and still achieve the required dynamic range and signal-to-noise ratio (SNR).

**LEVERAGING IP COMPONENTS** • The project’s time constraints were particularly severe, namely four months. Thus, they decided to rely on Cadence’s portfolio of silicon IP components—similar versions of these key blocks had already been proven on other designs, and in other technology processes.

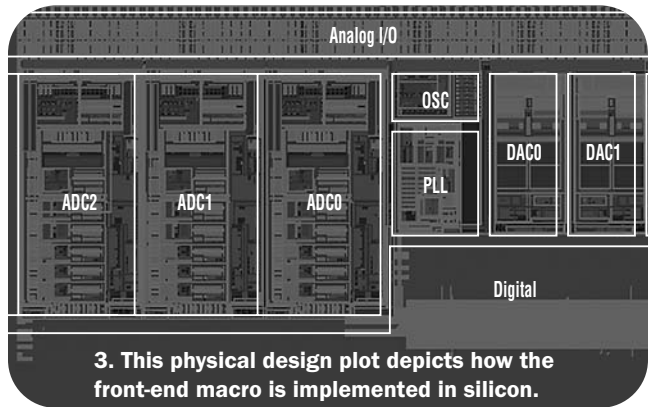
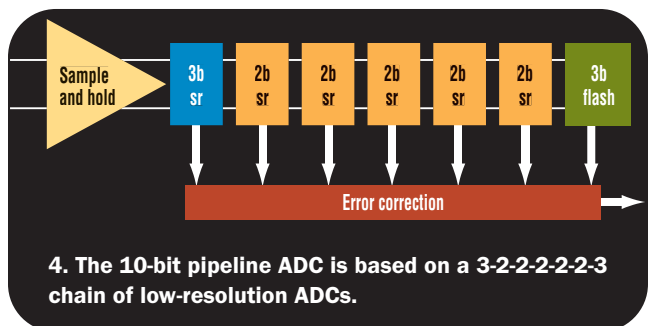


Figure 2 shows the analog front-end macro designed for the X-stream chip. The input to the front-end comes from four off-chip video tuners. Each tuner performs IF downconversion and filtering of the CATV signal, and delivers that input to an ADC on the X-stream chip. The ADC output is subsequently fed into a QAM demodulator and then decoded.

For high-end multimedia applications, such as demodulation of consumer-grade broadcast video, achieving high dynamic range and SNR is critical. The design team implemented 10-bit pipeline ADCs for each (CATV) input-channel, and 10-bit current-steering DACs for each (DOCSIS and OOB) output-channel. Therefore, key blocks in the analog front-end macro totaled six parallel 10-bit ADCs sampled at 25 MHz, two parallel 10-bit DACs clocked at 200 MHz, and a low-jitter PLL (to generate the reference-clock). All analog front-end circuitry was designed to operate at 3.3 V, while the digital core operated at 1.2 V.

To ensure good performance, the first concern of the design team was proper calibration/matching of signal gains across all input channels. In the case of the Digeo system, each input channel can be tuned independently. Not paying enough attention to channel-to-channel gain matching would cause intolerable variations in signal level among the six tuners being digitized and processed by the front-end chip. To ensure proper gain matching across all input channels, the design team made it possible for the pipeline ADCs to share a single common reference voltage, thereby minimizing gain mismatches between ADCs. For similar reasons, the design team added the capability to tie all DAC output current sources to a common reference as well.

Timing jitter (also called “aperture-uncertainty”) is a key



limiting factor in ADC performance. Small variations in the sampling instance can cause significant errors in the sampled voltage when the input signal is varying rapidly. Typically, designers must be concerned with two sources of jitter—random (e.g., caused by thermal or 1/f noise acting on the reference clock generator), and deterministic (e.g., caused by sources such as reference spurs from a PLL generating a clock, or a ripple on a power-supply voltage modulating propagation delays across clock trees).

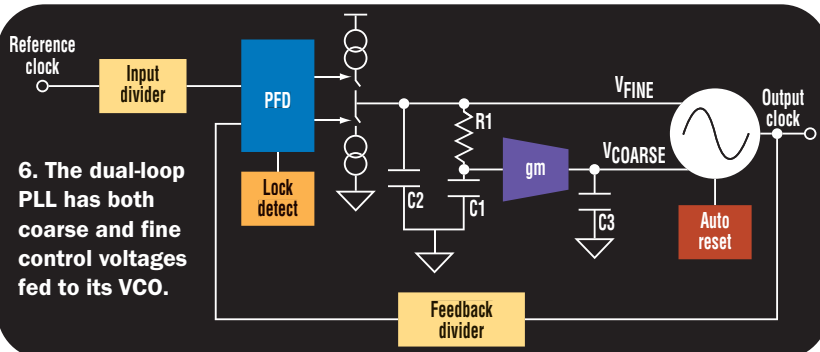
To minimize jitter, the design team employed balanced clock trees driven from a dedicated low-noise power domain to ensure simultaneous clocking of all ADCs and DACs. The clock signals were generated by using an on-chip, low-noise Pierce crystal oscillator to clock the ADCs directly (at 25 MHz). This low-noise clock was also used as a reference clock for a low-jitter, dual-loop PLL that multiplied the frequency (8X to 200 MHz) to clock the DACs (as well as the rest of the digital core).

In most mixed-signal ICs, the noise caused by switching digital portions of the chip can severely affect nearby analog and RF portions. For this reason, the chip floorplan was a key consideration. The partial IC floorplan in Figure 3 shows how the design team grouped the ADCs, I/Os, and DACs together within an analog macro, while isolating the over 15 million gates of digital logic within the lower portion of the floorplan.

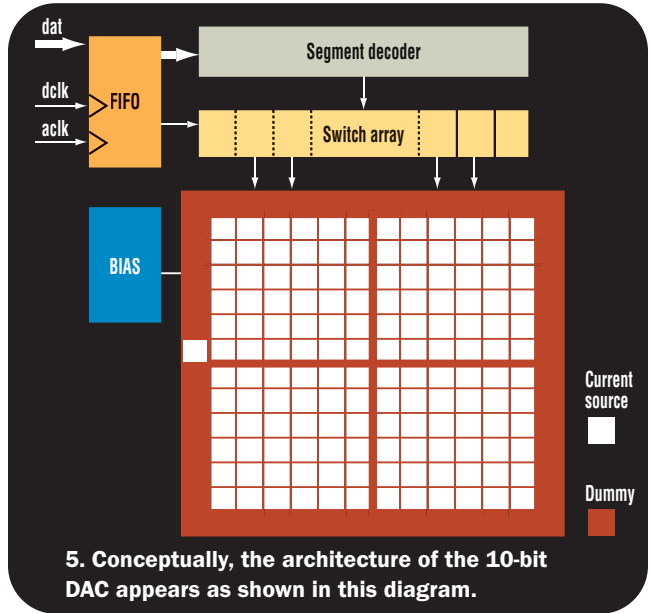
#### INDIVIDUAL FRONT-END ARCHITECTURE COMPONENTS •

Nonlinear behavior of the sample-and-hold (S/H) circuit is often the major source of distortion in an ADC, and can degrade performance significantly. In general, metal-oxide semiconductor (MOS) transistors exhibit source-drain channel resistance that varies as a function of gate-source voltage. When used as sampling switches, variations in the input signal level can slightly vary the sampling instant. This slight variation may cause significant distortion when sampling high-bandwidth signals.

A fairly well-known technique that counters this effect is to “bootstrap” a constant voltage (typically about  $V_{DD}$ ) across the gate-source terminals, when the gate is “on”.<sup>2</sup> This effectively shifts the input-signal voltage by a constant  $V_{DD}$ , thereby reducing the source-drain channel resistance to a point where it no longer varies with the input signal. Alternatively, whenever the gate is “off,” the gate is grounded and the switch is turned off as well. In this particular case, the design team decided to use a somewhat lower voltage than  $V_{DD}$  (2 V rather than 3.3 V)



**6. The dual-loop PLL has both coarse and fine control voltages fed to its VCO.**



**5. Conceptually, the architecture of the 10-bit DAC appears as shown in this diagram.**

to avoid overstressing the gate-oxide of the switch.

When designing ADCs, you’ll often run into a tradeoff between power consumption and size on the one hand, and linearity and “equivalent number of bits” (ENOB) on the other. Several alternative architectures exist for ADCs, each with its own advantages. High-speed, high dynamic-range applications will typically use direct-conversion (“flash”) ADCs (sampling rates as high as 1 to 2 Gsamples/s aren’t uncommon). However, flash ADCs have two major drawbacks: large size and heavy power consumption (due to the very large bank of comparators, which increase by 2X for each additional bit of resolution). In contrast, successive-approximation ADCs are very area-efficient (using a single comparator), but must work relatively slowly at high resolutions (typically less than 5 Msamples/s for 10 bits) due to the single comparator having to perform a separate comparison for each N bit of resolution.

A pipeline ADC essentially combines the best features of both these approaches by pipelining a chain of low-resolution ADCs to successively approximate the input signal. The multiple stages (seven total in our design: a 3-2-2-2-2-3 structure as shown in Figure 4) add latency as well as some additional silicon area. However, this good compromise between speed, silicon area, and power consumption makes pipeline ADCs one of the most popular types used today for applications requiring high resolution, high speed, low power, and small size.

**ACHIEVING ACCURACY •** To achieve overall 10-bit accuracy at 100 MHz, the dc gain of the op amp used in the first pipeline stage should be greater than 72 dB and settle to 0.1% accuracy within 4 ns. In this ADC design, a 3.3-V supply was chosen so that a 2-V, differential, peak-to-peak input dynamic range could maximize SNR. A larger signal swing is desirable to

achieve the required SNR in the face of degradation, which is caused by thermal noise and digital noise coupling in a large SoC through the substrate and in the packaging.

In addition, the ADC power is digitally controlled, enabling performance and power consumption to be optimized for different applications with sample rates ranging from 10 to 100 MHz. A digitally selected resistor works with an internal bandgap voltage to set the current in the subrange amplifiers. To operate at higher sample rates, the bias currents are increased to achieve faster settling. For lower sample rates, the bias currents are reduced to save power.

In the X-stream's 10-bit DACs, shown conceptually in Figure 5, the five LSBs are binary-weighted with current sources, and five MSBs are thermometer-coded with equal current sources 1 to 31. The architecture is a PMOS switching DAC similar to that described in the references.<sup>3</sup> The current-source-matrix device size, which is chosen to meet the strict 10-bit linearity requirement, is the dominant factor in determining the DAC layout area. Systemic errors are reduced in three ways:

1. The current-source matrix is laid out to be a double centroid to reduce thermal and stress gradient errors in the current-source matching. As the DAC code is incremented, the "on" current sources are evenly distributed around a central point so that variations due to

stress and temperature are averaged out.

2. A cascaded current source is used to obtain a higher output impedance to provide better spurious-free dynamic-range (SFDR) performance when generating high frequencies. This reduces variation in output current due to the load impedance.

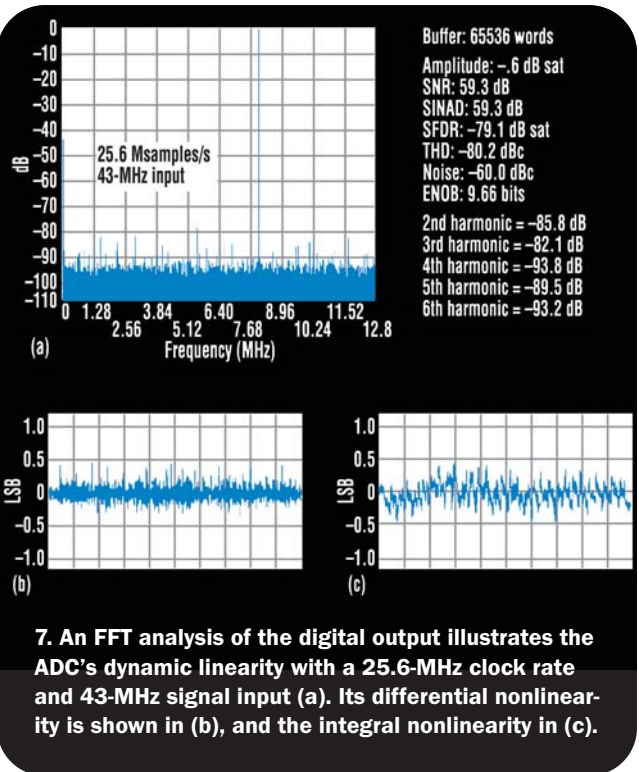
3. The voltage swing on the switch drivers is restricted. Reducing this voltage swing helps minimize clock feed-through and current fluctuation at the drain of the current sources.

A four-word-deep FIFO is used (essentially as a buffer) to receive the data words at the DAC's input. The noisy digital clock (dclk) writes the data into the FIFO, while a low-jitter analog clock (aclk, directly driven by the PLL) reads the data from the FIFO and clocks the final output flip-flops, which drive the DAC switch array.

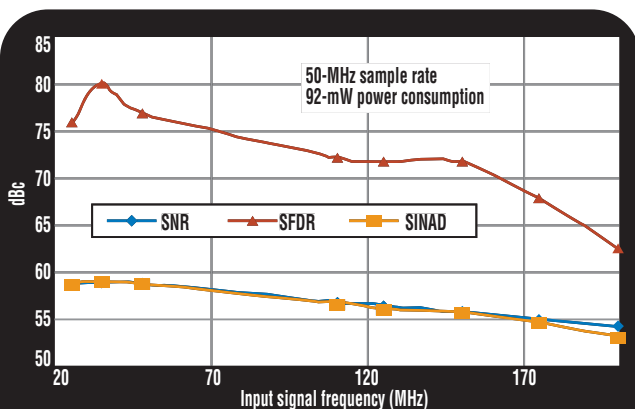
**DUAL-LOOP PLL ARCHITECTURE** • The PLL is perhaps the most important single component in terms of ensuring high

SNR. The performance of every DAC depends directly on the PLL generating a stable clock. In this design, the PLL multiplies the reference clock to provide a low-jitter, high-frequency clock. As shown in Figure 6, it uses a dual-loop architecture with two control voltages,  $V_{COARSE}$  and  $V_{FINE}$ , being fed to the VCO.

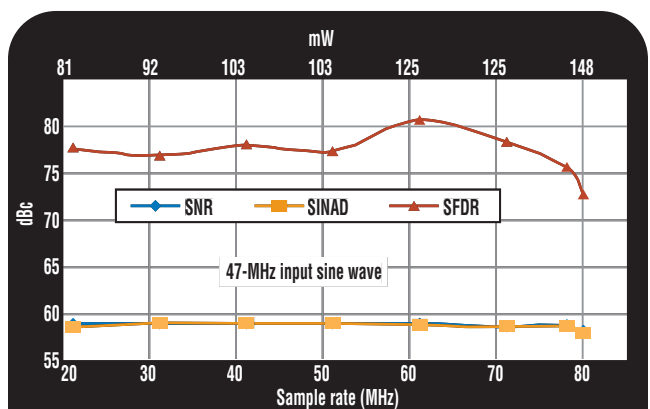
The first loop, the low-bandwidth, high-gain coarse control path, is used to track to the appropriate frequency and to



**7. An FFT analysis of the digital output illustrates the ADC's dynamic linearity with a 25.6-MHz clock rate and 43-MHz signal input (a). Its differential nonlinearity is shown in (b), and the integral nonlinearity in (c).**



**8. These plots illustrate the ADC's SNR, SINAD, and SFDR versus input frequency.**



**9. Here, the ADC's SNR, SINAD, and SFDR are plotted as a function of the sample rate.**

attenuate any VCO noise close to the output frequency. The wider-bandwidth, lower-gain second loop (the fine path) follows the conventional topology, transitioning from second order to first order before reaching the PLL bandwidth to ensure stability.

The coarse path is third order and must be attenuating before reaching the fine path's bandwidth. This is achieved with a gm-C filter. The PLL runs from a 1.2-V source that's regulated from 3.3 V to improve power-supply noise immunity; low-frequency disturbances on the 3.3-V supply are reduced by about 30 dB due to the gain of the regulator loop. At higher frequencies, the basic impedance of the pass device provides about 15 dB of attenuation of noise on the 3.3-V supply.

In this design, reference input frequency is 25 MHz and the output frequency is 200 MHz, with an effective loop bandwidth of between 1 and 2 MHz (depending upon process and temperature). For this block to be readily used in other applications, the VCO is designed to operate from 250 to 500 MHz, with an option to divide the output by two. The feedback divider, reference divider, and charge-pump current are programmable. Additional functionality includes PLL lock detection and an autoreset, which is an extra safeguard against VCO runaway.

The chip, which consisted of a mixed-signal front-end macro and multi-million-gate digital core, was fabricated using a 0.13- $\mu\text{m}$ , single poly, 1.2-V/3.3-V standard logic CMOS process, and a 400-ball BGA package. The analog I/O cells are located at the top of the chip; ADCs are placed on the left and DACs on the right.

The ADCs' dynamic linearity was measured by calculating an FFT of the digital output when a sinusoid is applied to the input. As shown in Figure 7, at 25.6 Msamples/s, with a 43-MHz sinusoid input, the ADC achieves 79 dBc SFDR, 59.3 dB SINAD, 0.5 LSB differential nonlinearity (DNL), and 0.5 LSB integral nonlinearity (INL)—with a total power consumption of 81 mW. This per-

formance implies the crystal oscillator/ADC combination features less than 1 ps RMS aperture jitter. Figure 8 shows the ADC performance as a function of input frequency at 50 Msamples/s. This ADC still achieves a SINAD of 53 dB with a 200-MHz sine-wave input. Figure 9 shows the ADC performance versus sample rate, in which the power consumption is tuned to the sample rate. (Corresponding values are listed on top of the figure.)

**EVALUATING ISOLATION** • Between the ADCs, the isolation is evaluated as follows: With ADC1's input terminated with a 50- $\Omega$  resistor, ADC0 and ADC2 sample a full-scale, 45-MHz input signal. By comparing ADC1's FFT when ADC0 and ADC2 are both on and off, the adjacent channel crosstalk is measured to be below 78 dBc. Further experimentation shows that the crosstalk appears to be dominated by the coupling in the package and on the test board.

This large multimedia IC with a multi-million-gate-count logic section demonstrates the feasibility of integrating multiple high-performance ADCs, DACs, and PLLs on an SoC, as well as the ability to achieve high levels of analog performance. Good isolation was attained between channels through careful package design, isolating power domains between analog channels on the IC, and employing a guard ring between the different blocks tied to its own ground pin.

Low-jitter clocking was achieved using an on-chip crystal oscillator. Special care was taken in clock routing with ground shields used between the clocks and sensitive analog nodes. On-chip separate power and ground domains for the circuitry used in each frequency domain helped reduce clock jitter further.

**ED Online 10815**

**WILLIAM EVANS**, system architect in the analog/mixed-signal RFIC Design Group at Cadence Design Systems, received his BS and MS degrees in electrical engineering from Lehigh University, Bethlehem, Pa.

**STEVE SVOBODA**, manager of technical marketing for engineering services at Cadence,

received BS degrees in both electrical engineering and economics from Johns Hopkins University, Baltimore, Md., and MS degrees in electrical engineering and engineering management from Stanford University, Calif.

**ANTHONY GRIBBEN**, analog/RF IC director at Cadence's Livingston, Scotland, facility, holds a BSc in electrical engineering and a PhD in microelectronics from Edinburgh University, Scotland.

References:

1. Farrand, Toby, "Digeo's X-stream Reference Platform," White Paper, Digeo Inc., May 2004
2. Abo, A. M., and Gray, P. R., "A 1.5V, 10-bit, 14.3-MS/s CMOS Pipeline Analog-to-Digital Converter," IEEE Journal of Solid-State Circuits, vol. 34, No. 5, p. 599-606, May 1999.
3. den Bosch, A.V., Borremans, M., Steyaert, M., and Sansen, W., "A 10-bit 1-Gsample/s Nyquist current-steering CMOS D/A converter," CICC, Proceedings of IEEE 2000, 21-24, May 2000, p. 265-268.