

DESIGN *FAQs*

Frequently Asked Questions:

HIGH-SPEED ADCs

Don Tuite, Analog/Power Editor

How fast is the current crop of high-speed analog-to-digital converters (ADCs)?

The pipeline architecture and silicon-bipolar and CMOS process technologies dominate commercial high-speed converters below 300 Msamples/s. Typical resolutions range from 12 to 14 bits. There's a large speed gap between 300 Msamples/s and 1 Gsample/s. The relatively few converters available above 1 Gsample/s have 8- or 10-bit resolution and use flash or folding/interpolating architectures in bipolar and CMOS process technologies. Currently, the fastest of these is a dual converter on a single chip that can be interleaved to achieve 3 Gsamples/s.

What are the application tradeoffs between speed and resolution in high-speed ADCs?

In test equipment, higher sample rates let designers measure wider ranges of signal frequencies and higher resolution in time. In communications, higher sample rates allow wider-bandwidth input signals to be digitized. On the other hand, resolution translates to dynamic range. Eight-bit resolution is

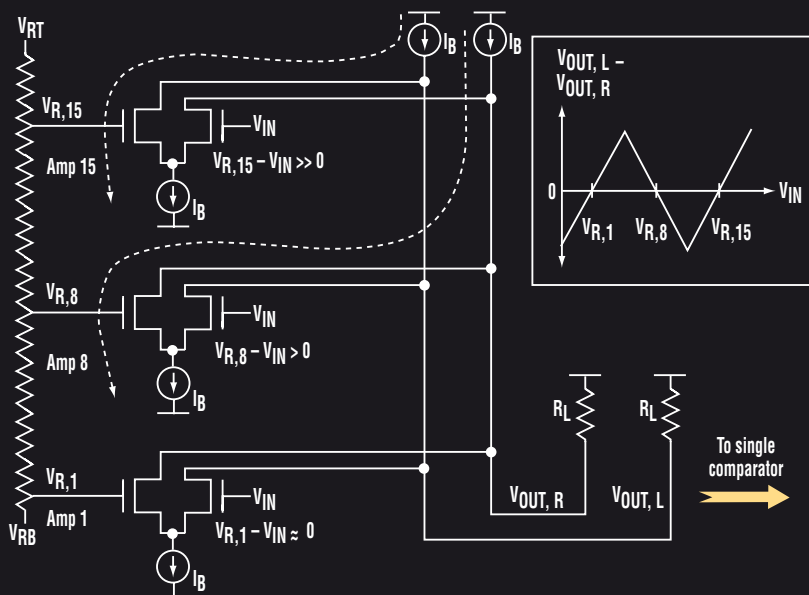
adequate for oscilloscopes, because it matches the typical display resolution. In contrast, spectrum analyzers need higher resolution and so use slower high-speed ADCs. In communications, very fast 8-bit converters are used in satellite and microwave point-to-point communications due to the fairly consistent signal strength in those applications. Slower, high-resolution ADCs are used in cellular basestations to deal with variations in signal strength between nearby and distant signal sources.

How does architecture affect speed?

Below 1 Gsample/s, most high-speed converters employ some variation in the pipeline architecture, in which parallel stages work on parts of successive samples. Shift registers align the bits from each stage in time and pass the combined sample on to error-correction logic. Above 1 Gsample/s, some converters implement the flash architecture, which uses large arrays of comparators to convert samples in a single step. Because an N-bit flash converter requires 2^{N-1} comparators, they're power-hungry and take up a lot of silicon die area. Introduced in 1993 but not widely commercialized, the folding/interpolating architecture reduces the number of comparators required and is responsible for CMOS's recent leap to multigigahertz speeds.

How did the folding/interpolating architecture suddenly get so fast?

It reached 800 Msamples/s by good design. Beyond that, the "single" ADCs (1 and 1.5 Gsamples/s) are actually interleaved dual devices on a common die. The latest chips contain a pair of the interleaved ADCs and can be themselves interleaved to achieve 2 and 3 Gsamples/s. Reaching these speeds wasn't easy. Interleaving often impacts performance because interdevice timing isn't consistent and gains and offsets do not necessarily match. Maintaining the potential speed gain required tight jitter and skew control and a considerable amount of on-chip calibration of gains, offsets, and timing.



In a folding architecture, the amplifier whose reference voltage is close to the input voltage is "active," while the two amplifiers not close to a crossing point are saturated and do not influence the comparator decision.

How does the folding/interpolating architecture work?

There are four aspects to the architecture: folding, interpolating, averaging, and calibration.

Folding preprocesses the analog input signal to map or fold it into sawtooth waveform, reducing the number of comparators required by the degree of folding. That is, for an 8-bit ADC with a folding factor of three, $(2^8 - 1)/3$, or 85 comparators are shared by three segments of the input voltage range. So, one comparator sees the outputs of three widely spaced amplifiers that are tied together with opposing polarities (see the figure). Cascading stages increases folding and further reduces the number of comparators required.

To recover the information lost in mapping or folding, additional "coarse" comparators are used to isolate which fold the input signal fell into. Because the coarse comparators work in parallel with fine comparators, there are no decision feedback loops, as in other non-flash architectures, making high-speed throughput possible.

With interpolation, cascaded pre-amplifier stages generate multiple "virtual" crossing points for every one "powered" crossing point. By allowing the generation of crossing points that aren't the result of the input crossing a physical reference voltage, interpolation reduces the required number of front-end amplifiers required.

What about averaging and calibration?

Averaging reduces the effects of device noise and offsets, including those introduced by folding. The output of each amplifier is superposed on its neighbor's outputs.

Folding is more sensitive to device offsets than flash, and CMOS pairs are harder to match than bipolars. The solution is to calibrate the preamp offsets. The chip designers matched gain and offset for the interleaved channels by sharing the same input buffer and including the track-and-hold in the calibration path. Using a common sampling clock took care of the sampling aperture offset between the channels.

ED Online 10862

PRODUCT Q&As

High-Performance Gigahertz-Speed ADCs

8-Bit, 1- to 3-GSPS ADC Family Performance (typical)

- 7.3 to 7.5 effective number of bits (ENOB) at Nyquist
- 1.75-GHz full-power bandwidth
- Bit error rate 10^{-18}
- DNL ± 0.25 LSB
- Crosstalk -71 dB
- Operating power of only 1 to 1.7 W (no heatsink required)

Features

- Interleaved dual-edge sampling (DES) mode enables up to 3-GSPS operation
- Choice of single or dual data-rate output clocking
- Multiple ADC synchronization capability
- Serial interface for extended control (gain, offset)
- Demultiplexed low-voltage differential-signaling (LVDS) outputs simplify data capture



The ADC081000/1500 (single) and ADC08D500/1000/1500 (dual) low-power, high-performance CMOS analog-to-digital converters (ADCs) digitize signals to 8-bit resolution at sampling rates up to 3 GSPS. Consuming a typical 1.7 W at 3 GSPS from a single 1.9-V supply, these devices are guaranteed to have no missing codes over the full operating temperature range.

High-Performance, Low-Power Gigahertz ADCs

Product	Description
ADC081000	8-bit, 1 GSPS
ADC081500	8-bit, 1.5 GSPS
ADC08D500	8-bit, dual, 500 MSPS (1 GSPS in DES mode)
ADC08D1000	8-bit, dual, 1 GSPS (2 GSPS in DES mode)
ADC08D1500	8-bit, dual, 1.5 GSPS (3 GSPS in DES mode)



For datasheets, online design training,
and more, visit us today at
www.national.com/adc
or call (800) 272-9959