

TABLE 2: PLATFORM AND STRUCTURED ASICs							
Vendor	Altera	AMI Semiconductor	ChipX	eASIC Corp.	Faraday Technologies	Fujitsu	NEC
Family/type of ASIC	HardCopy II; structured with 2 custom layers	XPressArray-II; structured with 5 custom layers	CX6000; structured with up to 4 custom layers	90-nm family; structured ASIC with 1 custom via layer	NetComposer; structured with 4 custom layers	AccelArray; platform with 4 custom layers	ISSP90 (STD/HIS); platform with 2 custom layers
Process technology	90 nm	150/250 nm (hybrid)	130 nm	90 nm	130 nm	110 nm	90 nm
Maximum logic speed/maximum usable gates/maximum programmable I/Os	350 MHz/2.2M/951	210 MHz/4.8M/1360	250 MHz/1.82/350	350 MHz/5.2M/852	300 MHz/1.15M/68	333 MHz/3.84M/1024	500 MHz/6.5M/900
Maximum embedded SRAM	8.8 Mbits	4.8 Mbits	1.75 Mbits	5.6 Mbits	1.0 Mbit	4.6 Mbits	5.7 Mbits
Maximum embedded PLLs/DLLs	12 PLLs to 1 GHz	8 PLLs to 800 MHz, 8 DLLs	7 PLLs to 1 GHz, multiple DLLs	10 PLLs to 1 GHz, 20 DLLs	5 PLLs to 1 GHz, 1 DLL	8 PLLs to 800 MHz	8 PLLs to 600 MHz, 42 DLLs
Embedded global/local clocks	16 global and 24 local	N/A	N/A	32 global	1 global and 10 local	8 global and 24 local	2 global and 128 local
Protocols supported in family*	SPI, SFI, XSBI, RapidIO, HyperTransport, NPSI, UTOPIA, PCI	PCI	USB, PCI	SPI, PCI	DMA, AMBA-AHB, I ² C, USB PHY, SMC, INTC, GPIO, Ethernet, PCI	RapidIO, SFI, Fibre Channel, SAS, SATA, SPI, HyperTransport, XAUI, CDR, NPSI, PCI, PCI Express	SPI, Ethernet (XAUI), POS-PHY Level 3, UTOPIA, 10GBASE, Fibre Channel, PCI, PCI Express
Programmable I/O standards supported*	LVTTL, LVCMOS, SSTL, HSTL, LVDS, LVPECL, PCI, PCI-X	LVTTL, LVCMOS, GTL, HSTL, SSTL, LVPECL, LVDS, PCI, PCI-X	LVTTL, LVCMOS, HSTL, SSTL, LVDS, RSDS, XOSC, PCI, PCI-X	LVTTL, LVCMOS, PCI, PCI-X, HSTL, SSTL, CTT, GTL, LVDS	PCI, PCI-X, LVTTL, LVCMOS	HSTL, LVCMOS, PCML, LVDS, SSTL, PCI, PCI-X	LVTTL, LVCMOS, LVDS, HSTL, PECL, SSTL2, PCI
External memory support	DDR1/DDR2, QDR2, RLDGRAM2, SDR	DDR1, QDR, RLDGRAM, ZBT	DDR1/DDR2	DDR1/DDR2	DDR1	DDR 1/2, QDR1/2, SDR, CAM	DDR1/DDR2
Other features	Embedded scan test, memory BIST, and Nios II Processor	Embedded scan test, memory BIST, and JTAG	Embedded scan test, memory BIST, JTAG, and PLL test bus	Embedded scan test, memory BIST, and JTAG	450-MHz, 32-bit ARMv4-compliant processor	Embedded scan test, memory BIST, JTAG, and PLL test bus	Embedded scan test, memory BIST, JTAG, and PLL test bus
“Drop-in IP” available	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Niche or unique feature	Only company to offer both FPGAs and structured ASICs, providing a simple migration path	Supports drop-in replacement IP for Xilinx Virtex-II/II Pro and Altera APEX-II/Stratix FPGAs	Full same-PHY migration support from development to structured to standard-cell ASICs	Customized with only a single via layer using ebeam technology that provides a zero-NRE solution	Addresses in-line Gbit Ethernet to Gbit Ethernet/PCI-X designs	Low power dissipation	Quick time-to-market at 90 nm

*For programmable I/O standards and protocols, the version and speed can be found on the vendor’s Web site.