

## Technology And Performance Tradeoffs For Various Multicore Technologies

Architecture	ARM11 MPCore	ARM Cortex-A9	SH-X3 (testchip)	Intel Core2 Duo	AMD X2	Sun Ultrasparc T1 ("Niagara 1")	Sun Ultrasparc T2 ("Niagara 2")	PPC 460S	AMCC "Titan"
	Arm		SH	x86	Sparc		Power		
<b>Threads per core</b>	1	1	1	1	1	4	8	1	1
<b>FPU</b>	Option per CPU	Option per CPU	Yes	Yes	Yes	Single FPU for 8 cores		Option	Yes
<b>Media processing engine</b>	No	Option: Neon	No	Yes: SSE	Yes: SSE	No	No	No	No
<b>True AMP (real time)</b>	Yes	Yes	Yes	No	No	No	No	No	Yes
<b>SMP (shared memory)</b>	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
<b>System coherence</b>	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
<b>Coherence at core speed</b>	Yes	Yes	No	Yes	No	No	No	No	Yes
<b>L1 cache-to-cache transfer</b>	Yes	Yes	WB snoop	Yes	No	Yes	Yes	No	No
<b>Coherence managed at L1 cache</b>	Yes	Yes	Yes	Yes	No	Yes	Yes	No	Yes
<b>L2 cache (shared/independent/either)</b>	Either	Either	n/a	Shared	Shared	Either	Either	Independent	Shared
<b>Out-of-order execution</b>	No	Yes	No	Yes	Yes	No	No	No	Yes
<b>Coherence technique</b>	Directory + snooping	Directory + snooping	Directory + snooping	Snooping	Snooping	Directory + snooping	Directory + snooping	Snooping	Snooping
<b>Cache maintenance propagation</b>	No	Yes	No	Yes	Yes	Yes	Yes	No	Yes