

POWER DESIGN FAQs

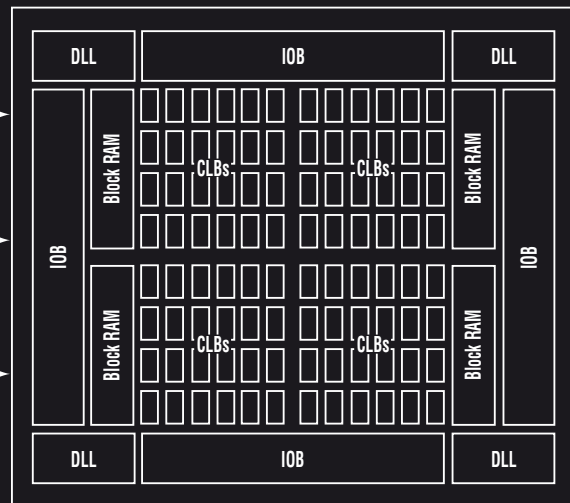
Frequently Asked Questions:

FPGA POWER MANAGEMENT

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What is an FPGA?

A field-programmable gate array (FPGA) is an IC that can include thousands of identical, programmable logic cells. A matrix of wires and programmable switches interconnects individual logic cells. A typical design involves specifying the simple logic function for each cell and selectively closing the switches in the interconnect matrix. FPGAs are primarily used to prototype an IC-based system. When the design is finalized, designers can convert the logic into hardwired ICs that operate at higher speeds. To operate properly, the FPGA must employ appropriate power-management technology.



Typical FPGAs include CLBs powered by V_{CCINT} , IOBs powered by V_{CCO} , delay-locked loops, and block RAM. V_{CCAUX} powers time-critical resources in some FPGAs.

What are the powering requirements for an FPGA?

FPGA power depends on the requirements of internal circuits. The FPGA has three major configurable elements: configurable logic blocks (CLBs), I/O blocks (IOBs), and interconnects (see the figure). The CLBs provide the functional logic elements. The IOBs provide the interface between the package pins and internal signal lines. The programmable interconnect resources provide routing paths to connect the inputs and outputs of the CLBs and IOBs onto the appropriate networks. The voltage applied to the CLBs (or core) is designated V_{CCINT} . V_{CCO} is the voltage supplied for IOBs. Some FPGAs have an additional voltage input designated as V_{CCAUX} .

What are typical voltage and current values for V_{CCINT} ?

Typical voltages are 1.2, 1.5, 1.8, 2.5, and 3 V, with currents up to 12 A. The larger the number of CLBs, the lower the voltage and higher the current. In addition, V_{CCINT} should rise monotonically, with no dip allowed.

What are typical voltage and current values for V_{CCO} ?

The most common V_{CCO} voltages are 1.2, 1.5, 1.8, 2.5, 3.3, or even 5 V in legacy systems. The current can range from 1 to 20 A.

What are the powering requirements for V_{CCAUX} ?

The typical auxiliary voltage (V_{CCAUX}) is 3.3 or 2.5 V. It powers time-critical resources in the FPGA, so it's susceptible to power-supply noise. V_{CCAUX} can share a power plane with V_{CCO} , but only if V_{CCO} does not have excessive noise.

What types of power sources can be used with an FPGA?

FPGA power-supply requirements include voltage outputs ranging from 1.2 to 5 V and current outputs from tens of milliamps to several amperes. The three possible approaches are a low-dropout (LDO) linear regulator, a switch-mode converter, and a switch-mode power module. The ultimate choice depends on the system, cost, and time-to-market requirements.

What are an LDO's advantages?

Use LDO regulators if board space is at a premium, low output noise is important, or the system requires a fast response to inputs and transients. LDOs provide low to medium output currents. An input capacitor typically cuts the inductance and noise on the input to the LDO. The LDO also requires a capacitor on the output to handle system transients and provide stability. Dual-output LDOs also can supply power for both the V_{CCINT} and V_{CCO} .

What are the advantages of switch-mode converters?

Switch-mode converters have an advantage when design efficiency is critical and the system requires large output currents. Switching supplies provide higher efficiency than LDOs, but their switching characteristics make their output more susceptible to noise. Unlike LDOs, switch-mode converters require inductors and possibly a transformer for dc-dc conversion.

What determines an FPGA's power consumption?

Consumption for CLBs includes

internal resources like the number of CLB logic cells/RAM block used, operation clock frequency, toggle rates, routing, and I/O power. For I/O power consumption, factors include output type, operating clock frequencies, number of outputs toggling at once, and output load. The actual power consumption depends on the specific system design.

What are the ramp-time requirements for an FPGA?

To ensure power-on, the core voltage V_{CCINT} ramp time must be in a specific range. For some FPGAs, excessive ramp times can yield longer-lasting power-on current because V_{CCINT} spends more time within the transistor turn-on threshold. Long power-on ramp time can cause thermal stress if the power supply provides a large current to the FPGA. Some dc-dc converters provide an adjustable soft start, permitting a ramp time controlled by an external capacitor. Ramp times depend on the FPGA manufacturer. Typical values are 50 to 100 ms.

Do you have to employ power-on sequencing for FPGAs?

Many FPGAs have no sequencing requirement, so V_{CCINT} , V_{CCO} , and V_{CCAUX} can be powered up simultaneously. When this isn't possible, the power-up current may be slightly higher. Sequencing varies with the specific FPGA. For some, it's important to apply power to the V_{CCINT} and V_{CCO} at the same time. For others, power supplies can turn on in any order. In most cases, powering up V_{CCINT} before V_{CCO} is a good practice.

Is inrush current a problem with FPGAs?

There's a power-on inrush current for some FPGA families when V_{CCINT} is within 0.6 to 0.8 V. During this period, the power converter supplies power continuously. Foldback current limiting isn't recommended in this application because the part reduces the output voltage to limit the current. But in current-limiting power solutions, once the circuit powered by the power supply with current limiting goes over a set current rating, the supply limits the current to that rating. **ED Online 9954**

PRODUCT Q&As

LOW-DROPOUT LINEAR REGULATORS FOR FPGAs AND DSPs

Employing CMOS process technology, National Semiconductor's two new series of low-dropout (LDO) linear regulators find applications as FPGA and DSP power sources. Additionally, they provide low-voltage conversion for powering notebook computers, enterprise servers, networking equipment, and battery-based systems. At its maximum-rated load current, the LP3884x series provides an ultra-low 75- to 210-mV (typical) dropout, and the LP3869x series provides dropout in the 250- to 450-mV (typical) range.

0.56-V OUTPUT DUAL-RAIL LDOs

The LP3884x series employs a bias voltage to achieve its ultra-low-dropout characteristics. This bias voltage is used to drive the gate of an internal NMOS power transistor, while its input voltage supplies power to the load. Unlike LDOs that have a bipolar pass element, LDOs using a CMOS architecture require significantly low quiescent current at any output load current. Use of an NMOS transistor also results in wide bandwidth and requires minimum external capacitance to maintain loop stability. The LP3884x series is stable with ceramic output capacitors, reducing footprint. It's also offered in fixed and adjustable output voltages and available in TO220 and TO263 packages with a -40°C to 125°C junction temperature range.



0.5-A/1.0-A CMOS LDO REGULATORS

Low-thermal-resistance LLP, SOT223, and TO252 packages house the LP3869x series, allowing full operating current to be used even in high ambient temperatures. This series uses an internal PMOS transistor that requires no dc base drive current for internal biasing. This enables ground current to remain below 100 μA , regardless of load current, input voltage, or operating temperature. These LDOs include thermal overload and current-limiting protection, and the LP38692 and LP38693 feature an enable pin that permits sequencing.

Product ID	I_{LOAD} (A)	V_{OUT} (V)	25°C V_{OUT} accuracy	Packaging
LP38841	0.8	0.8, 1.2, 1.5	1.5%	TO220-5, TO263-5
LP38842	1.5	0.8, 1.2, 1.5	1.5%	TO220-5, TO263-5
LP38843	3.0	0.8, 1.2, 1.5	1.5%	TO220-5, TO263-5
LP38841-ADJ	0.8	0.56 to 1.5	1.5%	PSOP-8
LP38842-ADJ	1.5	0.56 to 1.5	1.5%	PSOP-8
LP38690	1.0	1.8, 2.5, 3.3, 5.0	2.5%	TO252-3, LLP-6
LP38691	0.5	1.8, 2.5, 3.3, 5.0	2.0%	TO252-3, LLP-6
LP38692	1.0	1.8, 2.5, 3.3, 5.0	2.5%	SOT223-5, LLP-6
LP38693	0.5	1.8, 2.5, 3.3, 5.0	2.0%	SOT223-5, LLP-6
LP38690-ADJ	1.0	1.25 to 9	2.5%	LLP-6
LP38691-ADJ	0.5	1.25 to 9	2.0%	LLP-6
LP38692-ADJ	1.0	1.25 to 9	2.5%	SOT223-5, LLP-6
LP38693-ADJ	0.5	1.25 to 9	2.0%	SOT223-5, LLP-6



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